

Process Window Optimizer for pattern based defect prediction on 28nm Metal Layer

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ABSTRACT

At the 28nm technology node and below, hot spot prediction and process window control across production wafers have become increasingly critical. We establish proof of concept for ASML's holistic lithography hot spot detection and defect monitoring flow, process window optimizer (PWO), for a 28nm metal layer process. We demonstrate prediction and verification of defect occurrence on wafer that arise from focus variations exceeding process window margins of device hotspots. We also estimate the improvement potential if design aware scanner control was applied.

INTRODUCTION

Hot spot prediction and process window control across production wafers have become increasingly critical to prevent hotspots from becoming yield limiting defects. Traditional computational lithography applications are effective in eliminating major layout related issues before a mask is made, but are not directed towards predicting on-wafer performance, largely due to the unavailability of detailed data on actual process variations before tape-out. Process of record solutions to find these patterning defect locations are not sensitive enough or have low throughput and need improvements in order to be used as systematic defect detection tools.

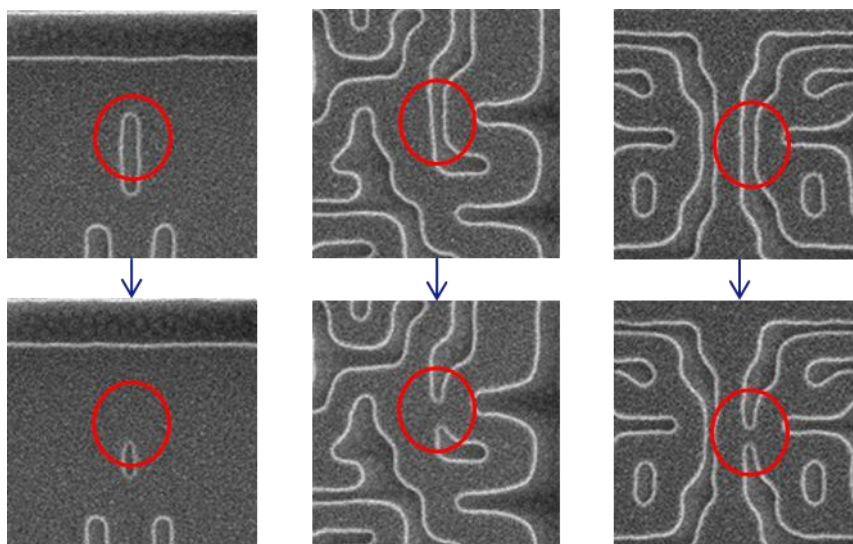


Figure 1: Even on product wafers focus variations can cause patterns to turn into real defects

Process Window Optimizer (PWO) extends the holistic lithography framework towards prediction, detection and verification of on-product patterning defects. The location of these process window limiting “hotspots” are determined using computational lithography simulations combined with on-product focus measurements and in-line scanner metrology. In this paper we demonstrate prediction and verification of defect occurrences on wafer that arise from focus variations approaching or exceeding process window margins of device hotspots.

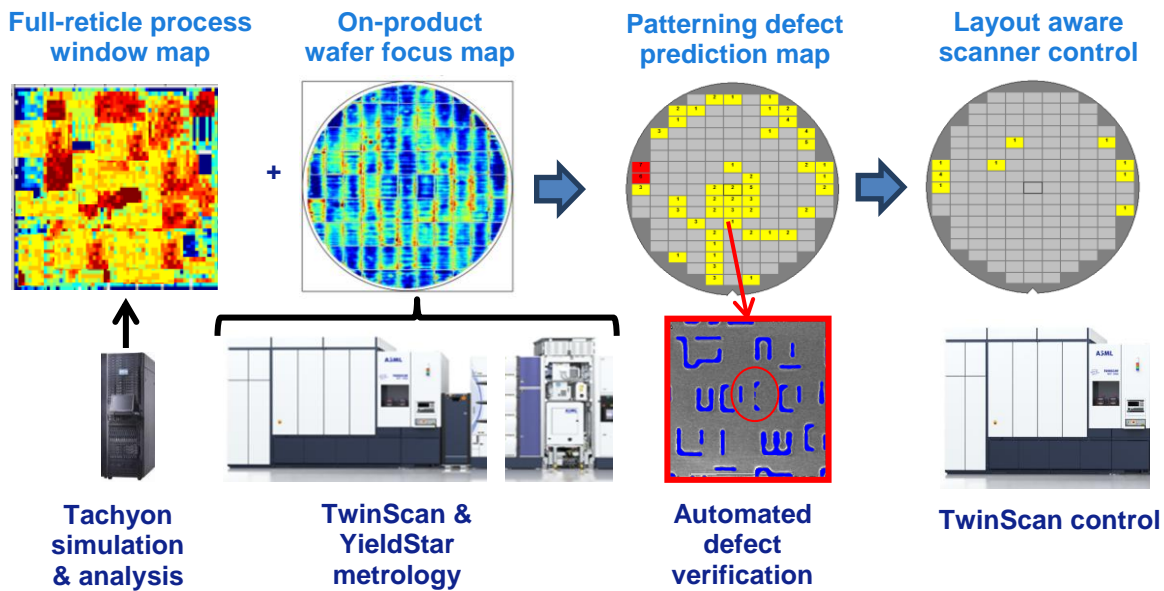


Figure 2: Holistic lithography concept for patterning defect prediction and layout aware scanner control [1]

Proof of concept has been demonstrated on a 28nm metal layer with a full-field product layout at STMicroelectronics. A three dimensional resist model (R3D)[2] was used to perform, resist-profile aware, simulations with the PWO software. The outcome of these simulations was used to predict the location of defects after etch. CD-SEM verification using Hitachi's contour extraction[3] for complex logic patterns is then shown. Focus variations are characterized by determining a systematic fingerprint that is combined with per-wafer topography data into dense focus maps to determine if and where across a production wafer focus-sensitive hotspots may turn into device defects.

Detecting the hot spots locations, with their CD estimations through focus can also help, to better control scanner focus correction in order to make sure that critical hotspots exposure are in their focus range. An estimation of this gain has been performed during this PWO evaluation.

TEST PLAN

A 28nm metal-1 product was selected to investigate the effectiveness of PWO at predicting defect locations. Each field was 26nm x 32.9 mm in size and consists of 7 different product blocks.

The exposures were performed on a NXT:1950i immersion scanner using short-flow wafers, with contact and metal stack only. This means that short-range topography effects from the front end of line will not influence the on-product focus measurements. These effects were studied in a separate paper [4].

Additionally, after etch, hotspot verification measurements were performed with a Hitachi CG 5000 and defect contours were extracted using the Hitachi contour extraction software. Extracted contours are analysed with PWO software to identify necking-type defects and quantify local minimum CDs. There was a significant delay between the exposure and etching of these wafers which meant that resist shrinkage occurred. To compensate for this effect a CD offset was applied to the measurement data.

Two PWO use cases were evaluated during this study. The first was computational defect prediction and control involving simulating the full chip process window and combining this with the effective focus map. The second was using pre-selected hotspots, combined with the effective focus map to predict the location of defects on the wafer, then verifying these results using CD-SEM measurements.

HYBRID DENSE FOCUS MAP GENERATION

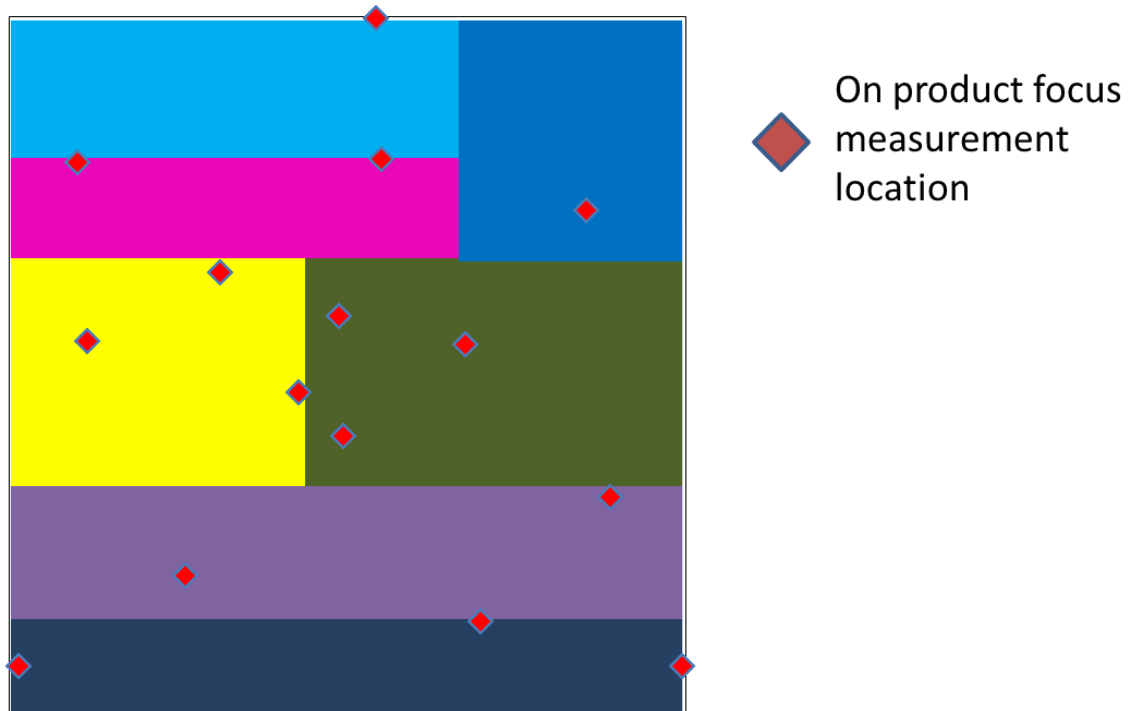


Figure 3: Field layout and on-product focus measurement locations of metal 1 product mask

An on-product focus map was generated using the multi wafer FEM methodology [5]. This step involves measuring focus sensitive isolated structures on the multiple product wafers exposed with a nominal focus delta between each wafer. Then re-constructing the Bossung curves for each measurement location and taking best focus as the Bossung top. For this, 15 locations per field were measured, after development (ADI), for every field. This method of determining best focus is only used for initial characterization, whereas diffraction based focus measurements would be used for inline focus measurements [6].

The hybrid dense focus map (HDFM) is generated using on-product focus measurements combined with scanner measurements on a higher spatial frequency. The scanner measurements are captured in-line and include the levelling non-correctable error (NCE) for every wafer and the lens image plane deviation (IPD). The levelling NCE is the residual which cannot be corrected by scanner levelling during wafer exposure and the lens IPD is a measurement of the focus offset induced by the lens across slit.

COMPUTATIONAL FULL CHIP DEFECT PREDICTION FLOW

The first step in the computational defect prediction flow is to find the patterns across the full chip that will limit the process window the most. Executing full field simulations across all focus conditions would take too much computation time. A method has been established in order to detect several locations that become simulated defects at worst focus conditions and, then, fine tune these locations in order to derive the most limiting hotspots. Once hot spots patterns are identified, pattern search and match across the field are performed in order to find all the pattern occurrences. Finally, CD through FEM for each hotspot was estimated by simulation.

From the hotspot list and data simulated, we generate a hotspot list together with two maps that characterize the product reticle in terms of Best Focus (BF) and Depth Of Focus (DOF). In order to build these BF and DOF maps, the reticle layout is split into 0.5x0.5mm pixels. The process limiting hotspots within each pixel are determined and the corresponding depth of focus and best focus is extracted. The combination of depth of focus and best focus tells us how much of a focus excursion is required to induce a defect at each location.

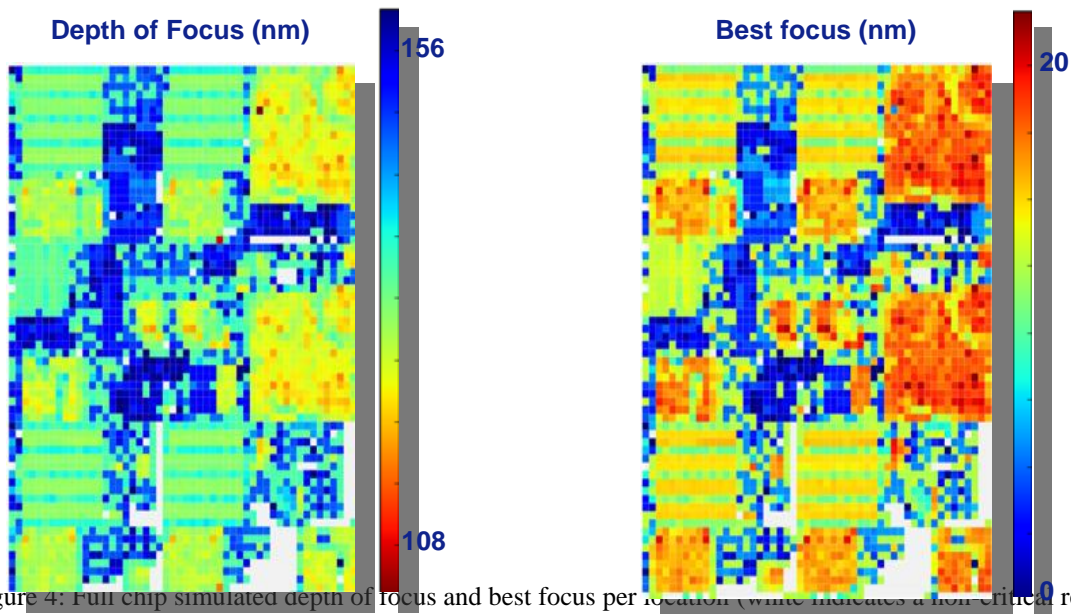


Figure 4: Full chip simulated depth of focus and best focus per location (white indicates a non-critical region)

The depth of focus of this product is most critical at the top right and center right of the field. These locations also have a higher best focus than the rest of the field. Optimizing scanner focus and levelling control to have a positive defocus at these locations may be a way to reduce defectivity.

The next step in the flow is to combine the simulated CD through FEM information with the effective focus values at hotspots locations in the hybrid dense focus map (HDFM). Wherever the defect CD for the corresponding wafer location focus fall below a given threshold (same as LMC threshold used for currently qualified verification in production), the hotspot will be flagged as a defect. A defect map was determined for each of the 9 wafers exposed through focus to visualize the increasing defectivity and induced defect locations at positive and negative focus.

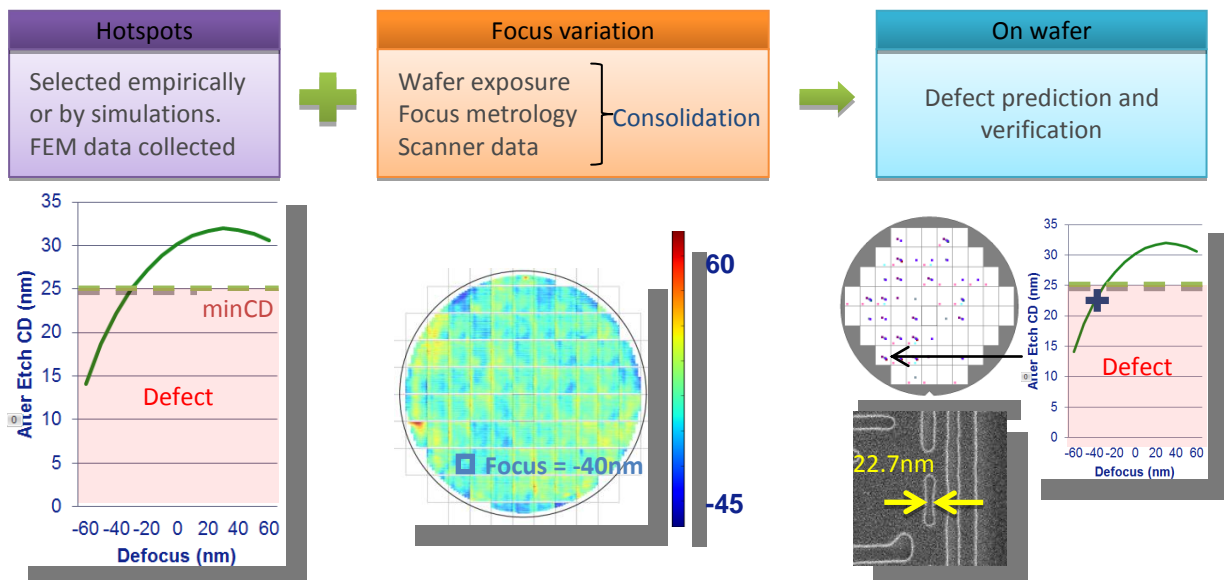


Figure 5: Simplified defect prediction flow

Predicted defect count is seen to increase as we move out of focus. Defects increase at a more rapid rate in negative defocus than positive defocus which can be considered for future process centering.

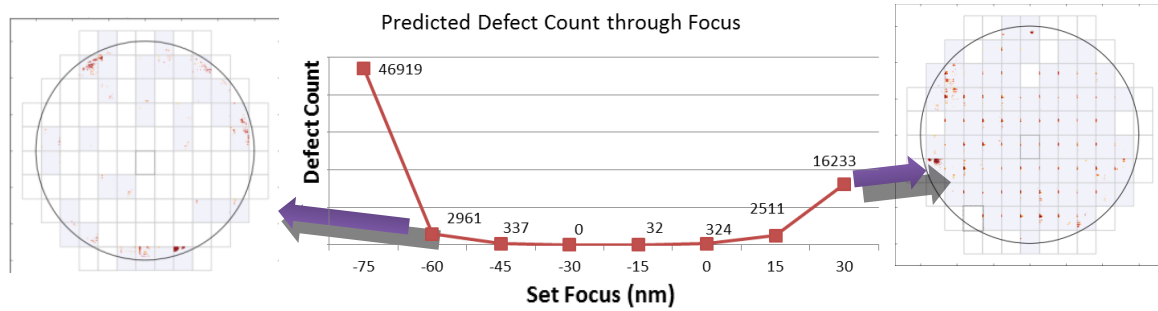


Figure 6: Predicted defect count and locations based on full chip simulation data

Using the overlapping process window information and the HDFM it was possible to generate a design aware scanner control output. This input aims to maximize the overlapping process window by applying focus corrections per exposure(z offset, Rx and Ry). The simulations show that a potential usable DOF improvement up to 17nm might be possible if correction was applied.

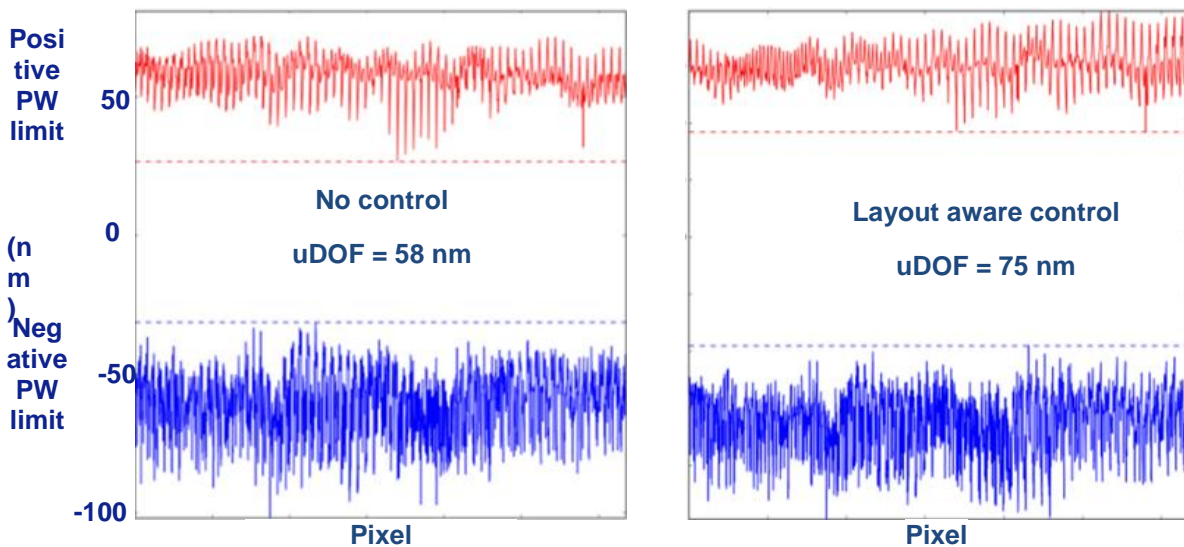


Figure 7: Simulated window comparison with and without PWO generated control recipe

Due to timing constraints it was not possible to verify the simulated defects on wafer in time for SPIE 2016. The complete computational full chip defect prediction flow is underway on a new test vehicle and will be presented in an upcoming conference.. The defect prediction and verification step will be presented in the next chapter using the user provided hotspot flow.

USER PROVIDED HOTSPOT FLOW

The user provided hotspot flow starts with the user selecting some known hotspots. These can be from simulation (standard LMC), measurement (process window qualification with bright field inspection tool) or empirically. For each of the 39 studied hotspots, we measured FEM data using CD-SEM image collection, combined with Hitachi contour extraction and applied ASML CD measurements to collect data through FEM. In order to select the most focus limiting hotspots, we ranked them and sorted out 7 hotspots kept for defect prediction.

Standard LMC is performed at worst process window conditions as opposed to PWO that will determine which hotspots are limiting the process window. LMC is performed at different focus and dose conditions with different resist heights (using Brion R3D resist profile calibrated models) defined as a standard and qualified production verification flow.

The focus offsets from the hybrid dense focus map at each position in the wafer are converted to predicted CD values, per hotspot, using the FEM curve. A hotspot is considered a defect if it falls below the CD defect threshold.

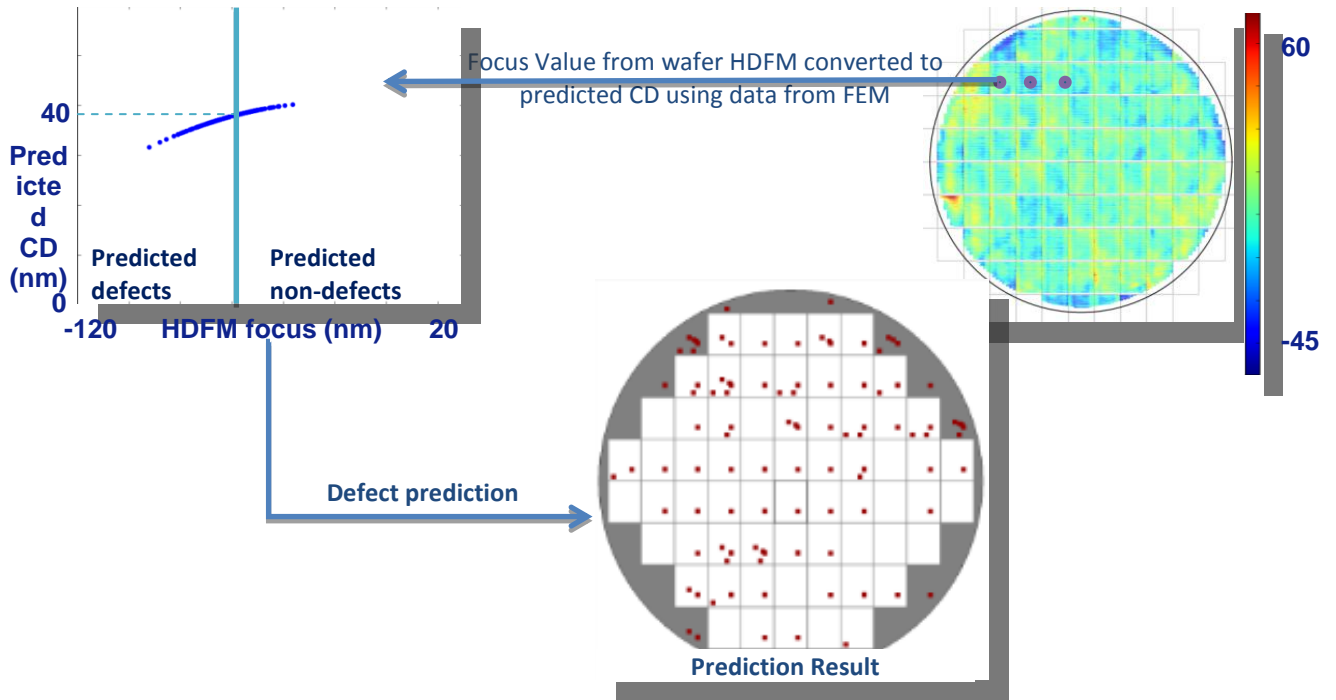


Figure 8: Defining defect and non-defect

In order to generate a significant occurrence of defects for evaluation purposes this study used an off-focus wafer. At -60nm set focus, defects are present sporadically across the wafer and at -90nm there are repeating defects in every field.

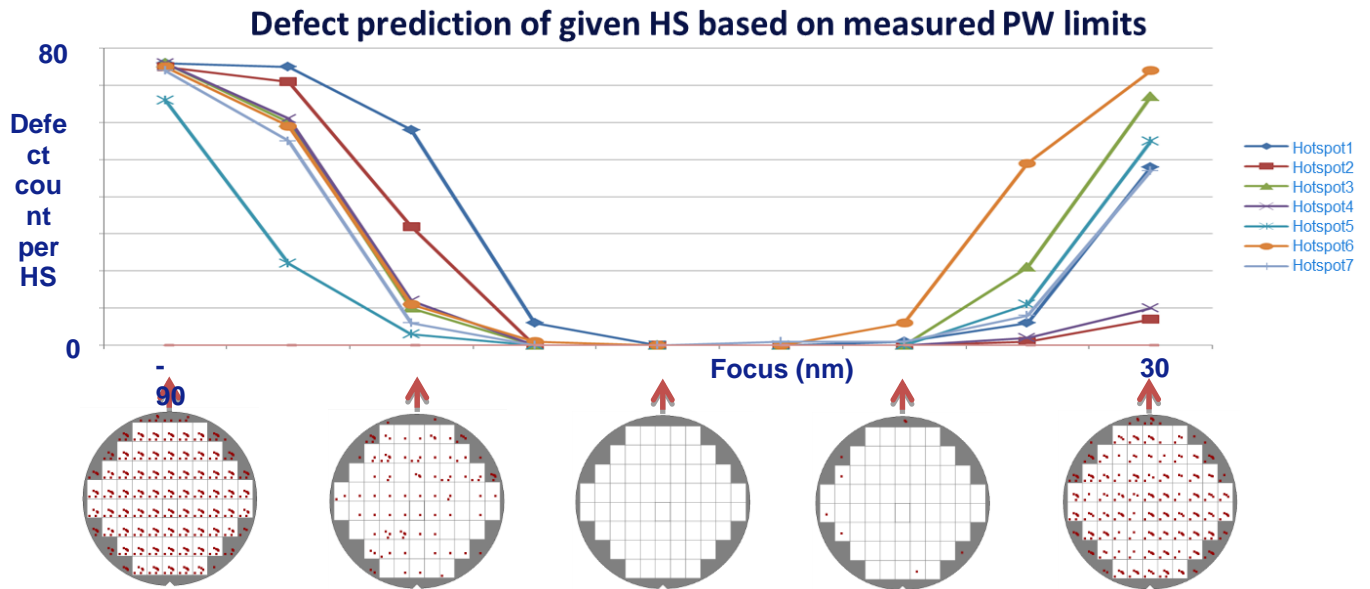


Fig 9: Defect prediction of given hotspots based on measured process window limiters

For this evaluation each hotspot location was measured. A check was done to see if the predicted defect locations the SEM revealed a defect or whether no defect was present. At predicted non-defect locations a check was also done to verify whether a non-defect was present or whether the simulation missed a defect location. The -75nm and -60nm set focus wafers were selected to check prediction accuracy.

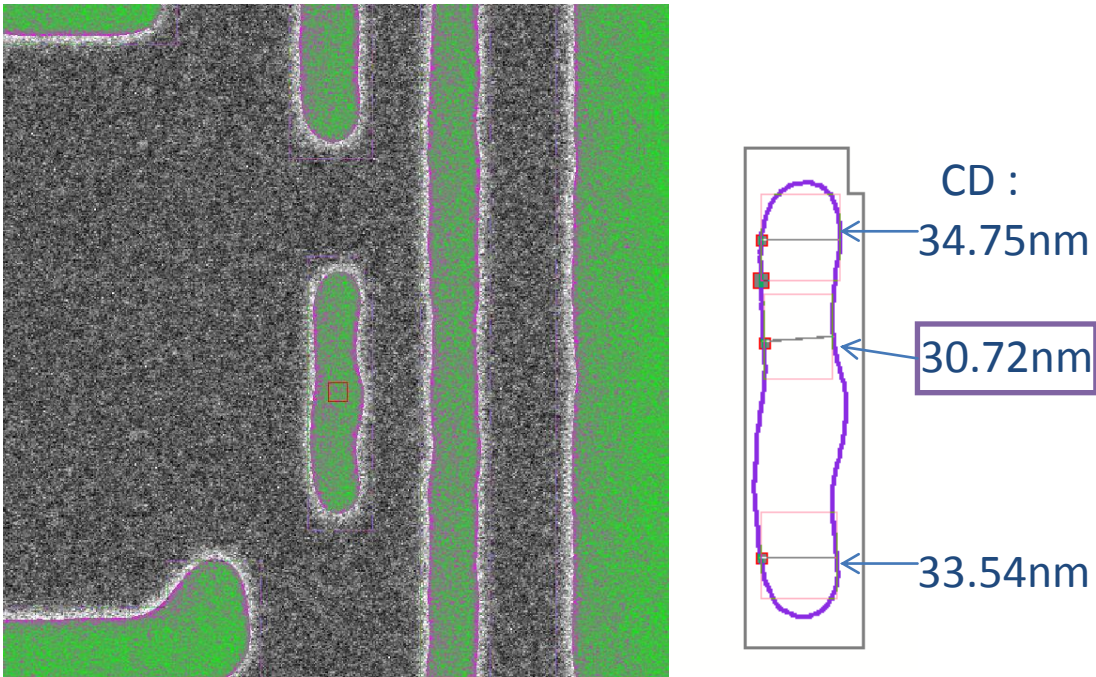


Figure 10: Example of neck location in contour extraction for selected hotspot

The defect measurements were performed, after etch using SEM. A contour was extracted from the measured images. Then LMC detectors were applied to check for defects. By applying a CD threshold to the LMC detector it is then possible to generate a binary yes/no defect state.

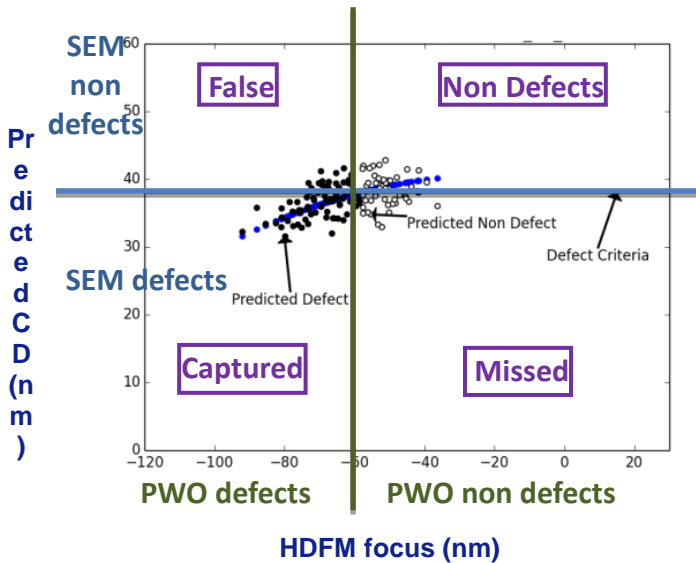


Figure 11: Visualization of PWO capture rate

Once measured CD data on CDU wafers are available, we were able to compare them to the predicted defects. The prediction accuracy is determined as a ratio of the number of accurate predictions with respect to the total number of hotspots. A matching location is also a requirement in order to have an accurate prediction.

$$\text{Capture rate} = \frac{\# \text{ Accurate predictions (captured or non defect)}}{\text{Total number of hotspots}}$$

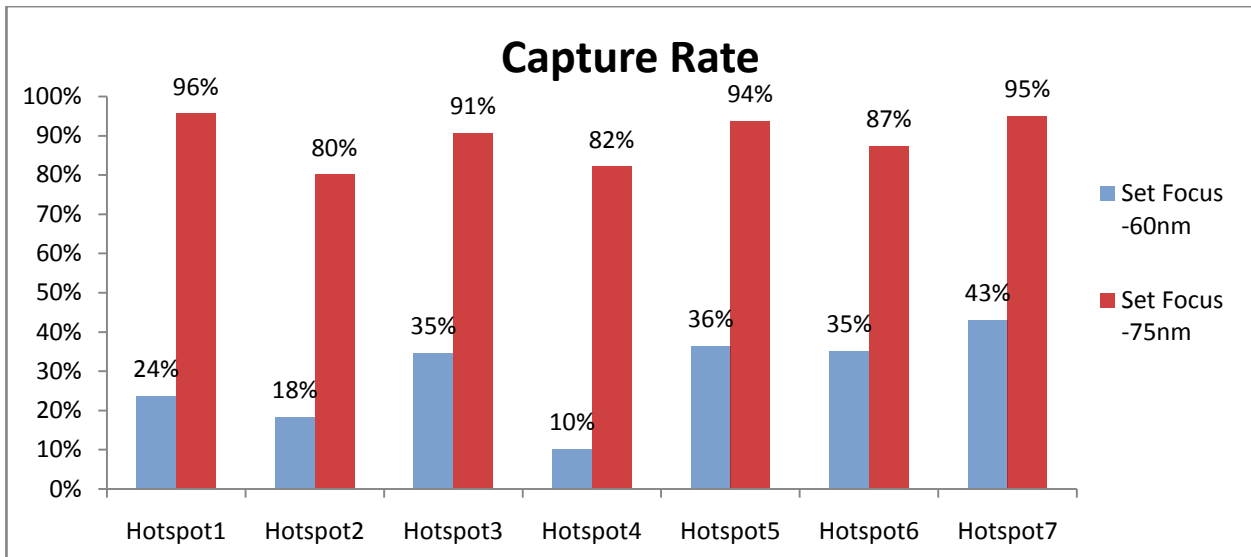


Fig 12: Capture rate of 8 user selected hotspots

The measured defect to predicted defect comparison gives an accurate capture rate. On the -75nm and -60nm wafers the average capture rate is 89% and 27%, respectively. An improvement of this metric would be expected using inline focus measurements to limit delay between lithography and etch. Including high frequent topography, etch fingerprint, mask and dose effects in the defect prediction is also expected to improve capture rate.

CONCLUSIONS

This evaluation has demonstrated the capability of using PWO from full chip layout layout to on-product defect prediction. A computational full chip simulation was combined with on product focus measurements and inline scanner metrology data to predict defect locations. Additionally, user selected hotspots were combined with the hybrid dense focus map and the prediction efficiency of PWO was investigated.

Resist simulation associated with inline data like dose and focusmap is a powerful way to predict patterning issues. PWO demonstrates this and opens a new area for patterning control. PWO will help us to improve our inline defect detection. It will accurately predict defect locations. These locations will be used in our defect detection tool to improve the signal to noise ratio. It will also enable a new way to adjust process within wafer and within field for a given layout. PWO can predict the defect count for several process adjustments and thus help us to find the best within wafer/within field process condition dose/focus to minimize patterning defects.

ACKNOWLEDGEMENTS

KEYWORDS:

Defect prediction, hotspots, focus, topography, simulation, process window, holistic lithography

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